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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,213	02/05/2001	William L. Betts	061607-1490	3031

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,213	BETTS, WILLIAM L.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,31-38,50-57 and 78-89* is/are pending in the application.

4a) Of the above claim(s) *78-89* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,31-38 and 50-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 78-89 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: claim 78 recites, "at least one memory element configured to receive a series of data inputs from the node and to store the series of data inputs for a delay period, wherein the delay period is set by a remote receiver", which is directed to synchronization properly classified in 714/789; claim 80 recites, "at least one memory element configured to receive a series of data input bits and further configured to output the oldest bit in the series after a delay of M symbol times", which is directed to synchronization properly classified in 714/789; claim 85 recites, "receiving, after a delay of M symbol times where M is greater than 1, a data input bit X(m+M) at a second symbol time m+M", which is directed to synchronization properly classified in 714/789; and claim 88 recites, "a serial-to-parallel converter configured to receive a first symbol in a first symbol period and a second symbol in a second symbol time separated from the first symbol time by M symbol periods, wherein the first symbol comprises a first plurality of bits and the second symbol comprises a second plurality of bits", which is directed to synchronization properly classified in 714/789. Note: claims 1-57 are properly classified in 714/774. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for

prosecution on the merits. Accordingly, claims 78-89 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

2. In view of the amendment filed 11/19/2004, the Examiner withdraws all objections to the claims.

Response to Arguments

3. Applicant's arguments filed 11/19/2004 have been fully considered but they are not persuasive.

The Applicant contends, "Ikeda in view of Davis does not disclose, teach, or suggest at least the feature of 'a portion of the plurality of logic calculators being capable of receiving a coefficient input' as recited in claim 1 or the 'means for receiving a coefficient input' as recited in claim 31 or 'logic for receiving a coefficient input' as recited in claim 50. The Office Action alleges that these features are disclosed by FIG. 1 of Davis. (Office Action, p. 7, paragraph 3). Applicant respectfully disagrees. FIG. 1 in Davis merely discloses a conventional convolutional encoder in which coefficients gl10-g1n and g20-g2n are connected to modulo 2 adders. Applicant respectfully asserts that Davis does not teach, disclose, or suggest that these coefficients are inputs or that they are received."

The Examiner asserts that that each of the modulo 2 adders 12 and 13 in Figure 1 of Davis are logic calculators; hence any one of the modulo 2 adders is a portion of the plurality of modulo 2 logic calculators for adding, being capable of receiving either coefficients gl10-g1n or coefficients g20-g2n as input to the modulo 2 adders 12 and 13 in Figure 1; hence coefficients gl10-g1n or coefficients g20-g2n are coefficient inputs to the logic calculators, i.e., modulo 2 adders 12 and 13. That is the logic calculators, i.e., modulo 2 adders 12 and 13 in Figure 1 are disposed to receive coefficient inputs gl10-g1n or coefficient inputs g20-g2n.

The Applicant contends, "Applicant respectfully asserts that even if Herzberg 'requires' an interleaver, Herzberg does not require a 'variable delay element' as recited in claim 16. Thus, even assuming, arguendo, that Khoury teaches this missing element, the Office Action has not provided a credible motivation for combining a variable delay element with the conventional interleaver disclosed in FIG. 4A of Herzberg".
The Examiner asserts that Figure 4-6 in Herzberg teach interleavers for convolutional codes. Figure 1 in Khoury as cited in the Examiner's last Office Action is a conventional Prior Art convolutional interleaver (col. 4, lines 59-60 in Khoury), which is typically used for convolutional codes. Figure 1 in Khoury substantially teaches the design characteristics of convolutional interleavers and one of ordinary skill in the art at the time the invention was made would have known that convolutional interleavers provide a means for overcoming burst errors for convolutional codes. The variable time delay in the convolutional interleavers is necessary for rearranging and interleaving data.

The Applicant contends, "Applicant respectfully submits that claim 57 is allowable for at least the reason that the proposed combination of Ikeda in view of Davis does not disclose, teach, or suggest at least the feature of 'a variable plurality of path memories' as recited in claim 57".

The Examiner asserts that claim 57 recites, "The system of claim 50, wherein a value of the variable delay is three bauds" and does not recite "a variable plurality of path memories" anywhere in the claim.

The Examiner disagrees with the applicant and maintains all rejections of claims 1-28,31-38 and 50-57. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 1-28,31-38 and 50-57 are not patentably distinct or non-obvious over the prior art of record in view of the references, Herzberg; Hanan (US 5996104 A) in view of Khoury; George (US 5912898 A) and Ross; Daniel P. (US 4901319 A) as applied in the last office action, filed 08/23/2004. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 31 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda; Yasunari et al. (US 6118825 A, hereafter referred to as Ikeda) in view of Davis; Robert C. (US 4545054 A).

See the Non-Final Action filed 08/23/2004 for detailed action of prior rejections.

5. Claims 1-7, 10-21, 24-28, 31-35, 38, 50-54 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzberg; Hanan (US 5996104 A) in view of Khoury; George (US 5912898 A).

See the Non-Final Action filed 08/23/2004 for detailed action of prior rejections.

6. Claims 8, 9, 22, 23, 36, 37, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzberg; Hanan (US 5996104 A) and Khoury; George (US 5912898 A) in view of Ross; Daniel P. (US 4901319 A).

See the Non-Final Action filed 08/23/2004 for detailed action of prior rejections.

Conclusion

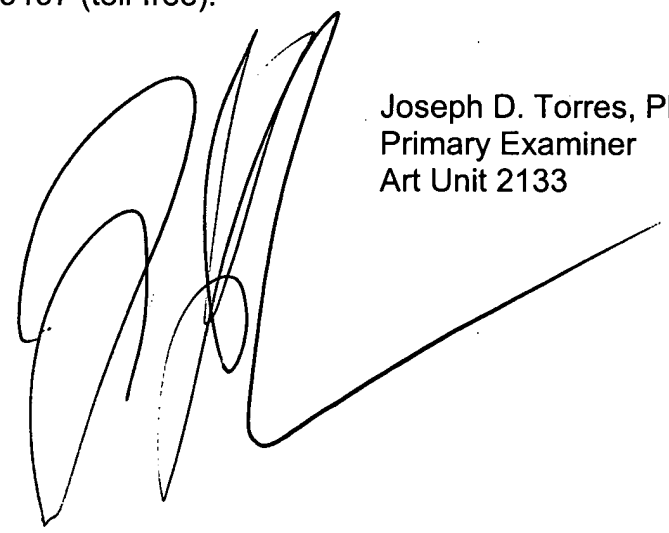
7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133